IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Method Of Forming Non-Volatile Resistance Variable Devices, Method Of Forming A Programmable Memory Cell Of Memory Circuitry, And A Non-Volatile Resistance Variable Device

* * * * *

INVENTORS

Kristy A. Campbell
John T. Moore

ATTORNEY'S DOCKET NO. MI22-1668

Method Of Forming Non-Volatile Resistance Variable Devices, Method Of Forming A Programmable Memory Cell Of Memory Circuitry, And A Non-Volatil Resistance Variable Device

TECHNICAL FIELD

This invention relates to non-volatile resistance variable devices, to methods of forming a programmable memory cell of memory circuitry and to non-volatile resistance variable devices.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metallization cell. Such a cell includes opposing electrodes having an insulating dielectric material

received therebetween. Received within the dielectric material is a fast ion conductor material. The resistance of such material can be changed between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a structural change at a certain applied voltage. With such voltage applied, a single conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions diffused therein. A specific example is germanium selenide having silver ions diffused therein. The present method of providing the silver ions within the

germanium selenide material is to initially chemical vapor deposit the germanium selenide glass without any silver being received therein. A thin layer of silver is thereafter deposited upon the glass, for example by sputtering, physical vapor deposition or other technique. An exemplary thickness is 200 Angstroms or less. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 500 nanometers. The thin nature of the deposited silver enables such energy to pass through the silver to the silver/glass interface effective to break a chalcogenide bond of the chalcogenide material. This may form Ag_2Se, which effectively dopes the glass with silver.

Saturation of silver in germanium selenide is apparently at a maximum of about 34 atomic percent or less depending on the germanium selenide stoichiometry. Yet, preferred existing technology for cell fabrication constitutes a concentration which is less than the maximum; in the case of 34 atomic percent maximum, an example concentration would be about 27 atomic percent.

After the chalcogenide material is provided with silver to a desired concentration, the top electrode material (typically silver) is next deposited. But, as the silver doping/diffusion into the chalcogenide material approaches the maximum or saturation, some Ag_2Se was discovered to form at the surface and remain there as opposed to diffusing into the glass. Further, the surface Ag_2Se was typically in the form of semicircular nodules or bumps anywhere from 50 Angstroms to 20 microns across. Unfortunately when the typical silver electrode material is subsequently deposited, such tends to mound on top of these previous bumps. This can create voids to the doped germanium glass

through the top electrode material, whereby the silver doped germanium selenide glass is partially exposed. Unfortunately, some of the photodeveloper solutions typically used for patterning the top electrode (i.e. tetramethyl ammonium hydroxide) will etch the glass that is exposed.

It would be desirable to overcome or at least reduce this problem. While the invention was principally motivated in overcoming this problem, it is in no way so limited. The artisan will appreciate applicability of the invention in other aspects unrelated to the problem, with the invention only being limited by the accompanying claims as literally worded and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes non-volatile resistance variable devices, methods of forming a programmable memory cell of memory circuitry and non-volatile resistance variable devices. In one implementation, a method of forming a non-volatile resistance variable device includes forming a first conductive electrode material on a substrate. An amorphous chalcogenide comprising material is formed to a first thickness over the first conductive electrode material. The chalcogenide material comprises A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof, and where "A" comprises at least one element which is selected from Group 13, Group 14, Group 15, or Group 17 of the periodic table. A metal comprising layer is formed to a second thickness over the chalcogenide material. The metal comprising layer defines or has some metal comprising layer transition thickness for the first thickness of the chalcogenide comprising material such that when said transition thickness is met or exceeded, said metal comprising layer when diffused within said chalcogenide comprising material transforms said chalcogenide comprising material from an amorphous state to a crystalline state. Yet, the second thickness is less than but not within 10% of said transition thickness. The metal is irradiated effective to break a chalcogenide bond of the chalcogenide material at an interface of the metal and chalcogenide material and diffuse at least some of the metal into the chalcogenide material, and said chalcogenide comprising material remains amorphous after the irradiating. After the irradiating, a second conductive electrode material is deposited over the

chalcogenide material, and which is continuous and completely covering at least over the chalcogenide material. The second conductive electrode material is formed into an electrode of the device.

In one implementation, a metal comprising layer is formed to a second thickness less than the first thickness over the chalcogenide comprising material. The metal is irradiated effective to break a chalcogenide bond of the chalcogenide material at an interface of the metal and chalcogenide comprising material and at least some of the metal is diffused into the chalcogenide comprising material, and said chalcogenide comprising material remains amorphous after the irradiating. The chalcogenide comprising material after the irradiating has a first region which is displaced from the interface at least by an interface region having a higher content of "A" than the first region. After the irradiating, a second electrode material is formed operatively proximate the chalcogenide material.

Other implementations and aspects are contemplated and disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metallization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless

otherwise indicated. Further, it will be appreciated by the artisan that "resistance variable device" includes devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the device's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A first conductive electrode material 16 is formed over dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. patents referred to above in conjunction with the preferred type of device being fabricated. A dielectric layer 18 is formed over first electrode material 16. Silicon nitride is a preferred example.

An opening 20 is formed through layer 18 to conductive electrode layer 16. Such is filled with an amorphous chalcogenide comprising material 22 to a first thickness, which in this example is essentially defined by the thickness of layer 18. By way of example only, an exemplary first thickness range is from 100 Angstroms to 1000 Angstroms. The chalcogenide comprising material comprises A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof, and where "A" comprises at least one element which is selected from Group 13 (B, Al, Ga, In, Tl), Group 14 (C, Si, Ge, Sn, Pb), Group 15 (N, P, As, Sb, Bi), or Group 17 (F, Cl, Br, I, At) of the periodic table. By way of example only, preferred elements for "A" are Ge and Si.

An example preferred method of forming material 22 over substrate 10 is by chemical vapor deposition to completely fill opening 20, followed by a planarization technique, for example chemical mechanical polishing. Material 22 is preferably formed to be amorphous and remains amorphous in the finished device.

A metal comprising layer 24 is formed to a second thickness over chalcogenide material 22. Exemplary metals, by way of example only, include silver, zinc and copper. In one embodiment, the second thickness is less than but not within 10% of a "transition thickness". Specifically, the material of the metal comprising layer defines or has some transition thickness for a given thickness of the chalcogenide material such that when said material transition thickness is met or exceeded, the metal comprising layer when diffused within said chalcogenide comprising material transforms said chalcogenide comprising material from an amorphous state to a crystalline state. Such transition thickness can be different for different stoichiometry chalcogenide materials and for different metals. Further, the second thickness is below but not within 50% of the transition thickness in one preferred embodiment, not within 65% in another preferred embodiment, and not within 85% in yet another preferred embodiment.

For example, and by way of example only, a metal layer consisting essentially of elemental silver received over a 500 Angstrom germanium selenide glass having 25% atomic germanium and 75% atomic selenide has a transition thickness of 140 Angstroms. Accordingly in one preferred embodiment in such

example, a metal layer 24 consisting essentially of elemental silver will have a thickness less than 124 Angstroms (i.e., not within 10%), in another embodiment a thickness less than 70 Angstroms (i.e., not within 50%), in another embodiment a thickness less than 49 Angstroms (i.e., not within 65%), and in another embodiment a thickness less than 21 Angstroms (i.e., not within 85%).

Referring to Fig. 2, metal 24 is irradiated effective to break a chalcogenide bond of the chalcogenide material at an interface of metal 24 and chalcogenide material 22, and diffuse at least some of metal 24 into chalcogenide material 22, with chalcogenide comprising material 22 remaining in the amorphous state after the irradiating. In Fig. 2, material 22 is designated with numeral 23 and peppered in the drawings to indicate metal ions being received therein. A preferred irradiating includes exposure to actinic radiation having a wavelength from about 164 - 904 nanometers, with radiation exposure at between 404 - 408 nanometers being a more specific example. A more specific example is a flood UV exposure tool operating at 4.5 milliwatts/cm^2 energy for 15 minutes in an oxygen-containing ambient at room temperature and pressure. A mechanism of incorporation might include Ag_2Se formation at the chalcogenide surface/interface, and diffusion doping thereof into material 22.

All of material 24 received directly over chalcogenide comprising material 22 might be diffused to within such material as shown, or only some portion thereof might. The thickness of layer 24 is also chosen to be suitably thin to enable the impinging electromagnetic radiation to essentially transparently pass through material 24 to the interface of such material with chalcogenide

material 22. The exemplary preferred thickness is as described above in comparison with the thickness of chalcogenide material 22, and is preferably less than or equal to 200 Angstroms.

The apparent linear thickness of layer 24 as a percentage of the linear thickness of chalcogenide material 22 effectively results in the same approximate metal incorporation in atomic percent within the chalcogenide material. In other words, a 2% to 20% thick metal layer compared to that of the underlying chalcogenide material will result in metal incorporation of an atomic percent of from about 2% to about 20% respectively. Accordingly as compared to conventional prior art, a lower atomic percent incorporation is conducted to within the chalcogenide material, and has been discovered in preferred embodiments to result in the elimination of surface agglomeration of Ag_2Se which is understood to have principally caused the discontinuous subsequent electrode formation of the prior art. Thereby in the preferred embodiment, a continuous, void-free, complete covering of a subsequently deposited electrode layer was achieved in connection with deposition over at least chalcogenide material 23, as further described below.

In one exemplary embodiment, layer 24 of metal is formed to a second thickness over the chalcogenide material and the irradiating is effective to produce the chalcogenide material 23 (Fig. 2) to have an interface region 25 and a first region 23 which is displaced from the interface of the metal and chalcogenide material by interface region 25. In this exemplary embodiment, interface region 25 is characterized by a higher content of "A" of the A_xB_y

material as compared to the content of "A" in first region 23. Apparently, photodoping or other irradiation doping to the stated lower second thicknesses can result in greater driving of silver or other metal into germanium selenide or other glasses which can result in an outer germanium rich layer of the glass. This may facilitate a preferred lack of surface agglomeration of Ag_2Se.

Interface region 25 is preferably formed to have a thickness of less than or equal to 100 Angstroms. Further, such is preferably formed to have a thickness of at least 10 Angstroms. Further preferably, interface region 25 and first region 23 are formed to have substantially the same concentration of the diffused metal. Further preferably, interface region 25 and first region 23 are respectively homogenous.

Referring to Fig. 3, after the irradiating, a second conductive electrode material 26 is deposited over chalcogenide material 23. In the preferred embodiment, such second conductive electrode material is continuous and completely covers at least over chalcogenide material 23. An example preferred thickness range for second electrode material layer 26 is from 140 Angstroms to 200 Angstroms. The first and second conductive electrode materials might be the same material(s), or different material(s). By way of example only, preferred top and bottom electrode materials include silver, tungsten, platinum, nickel, carbon, chromium, molybdenum, aluminum, magnesium, copper, cobalt, palladium, vanadium, titanium, alloys thereof and compounds including one or more of these elements. In accordance with a preferred programmable metallization cell embodiment, and where "A" is Ge, at least one of materials

16 and 26 comprises silver. During formation of layer 26, some of it might diffuse into layer 23. Layer 26 and any remnant material 24 received directly over chalcogenide material 23 will constitute one electrode of the resistance variable device being fabricated, with layer 16 constituting another or second electrode for the device.

Referring to Fig. 4, materials 24 and 26 are patterned into an electrode 30. Patterning to produce electrode 30 is typically and preferably conducted utilizing photolithography. Such provides but one preferred example of forming a second electrode material operatively proximate the chalcogenide material. In a preferred embodiment, such results in the formation of a non-volatile resistance variable device which is fabricated into a programmable memory cell of memory circuitry. In one preferred embodiment, the device is finally formed to have a concentration of metal in chalcogenide material 23 of less than 30% atomic in a lowest of a plurality of variable resistance states.

Referring to Fig. 5, one or more dielectric layers 32 are ultimately formed over the device. Of course, intervening conductive and semiconductive layers might also be provided to form other lines and devices outwardly of the depicted device.

Independent of the method of fabrication, the invention comprises a non-volatile resistance variable device comprising some substrate having a first electrode formed thereover, for example electrode 16. A resistance variable chalcogenide material 23 having metal ions diffused therein is received operatively adjacent the first electrode. A second electrode, for example

electrode 30, is received operatively adjacent the resistance variable chalcogenide material. The chalcogenide material comprises A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof, and where "A" comprises at least one element which is selected from Group 13, Group 14, Group 15, or Group 17 of the periodic table.

The second electrode and resistance variable chalcogenide material operatively connect at an interface. The chalcogenide material has a first region 23 which is displaced from the interface at least by a chalcogenide material interface region 25 having a higher content of "A" than first region 23. Preferably and as shown, first region 23 extends to first electrode 16.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.